REMARKS

Claims 1 and 3-20 are all the claims presently pending in the application. Claims 1, 3, and 20 have been amended to clarify the invention. Claims 3-19 have been withdrawn from prosecution, but are subject to rejoinder upon the allowance of the elected claims. Of the remaining claims, claims 1 and 20 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicants also note that, notwithstanding any claim amendments herein or later during prosecution, Applicants' intent is to encompass equivalents of all claim elements.

Claims 1 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Houlihan, et al. reference (U.S. Patent No. 6,258,673 B1) in view of the Baumann reference (U.S. Patent No. 5,866,445).

This rejection is respectfully traversed in the following discussion.

I. THE RESTRICTION REQUIREMENT

First, Applicant respectfully submits that the Examiner has failed to further prosecution of the present application by failing to comply with the requirements of the M.P.E.P.

In particular, the Examiner fails to answer the substance of the Applicants' traversals.

The M.P.E.P. states:

"Where the applicant traverses any rejection, the examiner should, if he or she repeats the

rejection, take note of the applicant's argument and answer the substance of it." (Emphasis added, M.P.E.P. § 707.07(f))

In this instance, in the remarks of the Amendments that were filed on August 20, 2003 and on February 18, 2004, the Applicants pointed out that the Examiner's restriction requirement was prima facie insufficient because of the failure to show a serious burden on the Examiner to search and examine the claims of the entire application in accordance with the requirements set forth in § 803 of the M.P.E.P.

The Examiner continues to ignore this traversal and has, thereby, failed to answer the substance of the traversal in clear violation of the requirements of the M.P.E.P.

Applicants hereby incorporate those traversals herein again in their entirety and respectfully request that the Examiner either: 1) withdraw the restriction requirement; or 2) answer the substance of the traversal.

Secondly, Applicants thank the Examiner for indicating that the non-elected claims will be rejoined upon indication of allowance of the elected claims since the non-elected claims include all the limitations of the elected claims.

II. THE CLAIMED INVENTION

An exemplary embodiment of the claimed invention is directed to a semiconductor device that includes two first MOSFETs each having a first gate oxide film, a second MOSFET having a second gate oxide film that is thicker than the first gate oxide film, and a third MOSFET of a p-type having a third gate oxide film which is thicker than the first gate oxide film and is thinner

than the second gate oxide film. The second MOSFET and the third MOSFET form a first single CMOS pair and the two first MOSFETs form a second single CMOS pair.

The present invention is a configuration that provides two CMOS pairs which can achieve high speed operation, high reliability and low consumption power using suitable gate oxide film thicknesses. This is a non-trivial matter because, as the inventors discovered, n-type and p-type MOSFETs operating with the same threshold level have gate-channel leakage current characteristics which are different from each other.

Thus, the inventors discovered that the thickness of the gate oxide film of the p-type MOSFET does not need to be equal to that of the n-type MOSFET. To the contrary, the inventors discovered that the thickness of the gate oxide film of the p-type MOSFET may be thinner than that of the complimentary n-type MOSFET in a single CMOS pair because the leakage current of the p-type MOSFET is one order of magnitude smaller than that of the n-type MOSFET. Additionally, the thinner gate oxide film of the p-type MOSFET increases the operating speed.

The present invention provides a first CMOS pair having higher threshold MOSFETs and a second CMOS pair having lower threshold MOSFETs. The lower threshold MOSFETs having a common gate oxide film while the higher threshold MOSFETs each have thicker gate oxide films, with the nMOS having a thicker gate oxide than the pMOS.

III. THE PRIOR ART REJECTION

The Examiner alleges that the Baumann reference would have been combined with the

Houlihan et al. reference to form the claimed invention. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Firstly, Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, the Houlihan et al. reference is directed to avoiding the pitfalls of a first conventional method of requiring multiple HF etches (col. 1, lines 18-25) and a second conventional method of relying solely upon nitrogen implantation (col. 1, lines 26-32) to provide different gate oxide film thicknesses for generic transistors by combining aspects of each of these conventional methods (col. 2, lines 11-57).

In contrast, the Baumann reference is specifically directed to the completely different and unrelated asymmetry problem in PMOS and NMOS drive currents in a CMOS transistor pair without adversely affecting silicon real estate (col. 1, lines 11-45).

One of ordinary skill in the art would not have been motivated to modify the disclosure of the Houlihan et al. reference based upon the teachings of the Baumann reference. The Houlihan et al. reference is concerned with avoiding the pitfalls of a first conventional method of requiring multiple HF etches and a second conventional method of relying solely upon nitrogen implantation. Thus, since the Baumann reference is not concerned with avoiding the pitfalls of a first conventional method of requiring multiple HF etches and a second conventional method of relying solely upon nitrogen implantation, one of ordinary skill in the art would not have referred

to the Bauman reference in an attempt to solve this problem.

Further, the Baumann reference is only concerned with addressing the asymmetry problem of CMOS transistor pairs. Since the Houlihan et al. reference is not concerned with addressing the asymmetry problem, one of ordinary skill in the art would not have been motivated to combine these references.

Indeed, as explained previously, the Houlihan et al. reference does not teach or suggest anything at all regarding CMOS transistor pairs, let alone how to address the asymmetry problem of CMOS transistor pairs.

Further, Applicants submit that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner.

The Examiner alleges that the Houlihan et al. reference and the Baumann reference are from the same field of endeavor of CMOS semiconductor devices, and that, therefore, the purpose disclosed by the Baumann reference would have been pertinent to the disclosure of the Houlihan et al. reference.

However, contrary to the Examiner's allegation, and as explained above, and earlier, the Houlihan et al. reference does not teach or suggest a CMOS transistor pair. Thus, the purpose of addressing the asymmetry within a CMOS transistor pair is not pertinent to the disclosure of the Houlihan et al. reference since the Houlihan et al. reference does not teach or suggest a CMOS transistor pair.

Further, while the Baumann reference appears to disclose a CMOS pair. The Baumann reference, does not provide any motivation to modify anything to include a CMOS pair.

In summary, the Examiner's entire premise for alleging that one of ordinary skill in the art would have been motivated to modify the disclosure of the Houlihan et al. reference based upon the disclosure of the Baumann reference is based entirely upon false pretenses.

Moreover, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention.

None of the applied references teaches or suggests the combination of features of the present invention including two first MOSFETs having a common first gate oxide film, a second MOSFET having a second gate oxide film thicker than the first gate oxide film, and a third MOSFET of a p-type having a third gate oxide film which is thicker than the first gate oxide film and is thinner than the second gate oxide film, wherein the second MOSFET and the third MOSFET form a first single CMOS pair, and wherein the two first MOSFETs form a second CMOS pair.

While the Houlihan et al. reference appears to disclose transistors having different gate oxide thicknesses, these transistors are merely on the same substrate. The Houlihan et al. reference does not teach or suggest providing: 1) two first MOSFETs having a common first gate oxide film; 2) a second MOSFET having a second gate oxide film thicker than the first gate oxide film, and a third MOSFET of a p-type having a third gate oxide film which is thicker than the first gate oxide film and is thinner than the second gate oxide film, wherein the second MOSFET and the third MOSFET form a first single CMOS pair; and 3) wherein the two first MOSFETs form a second CMOS pair.

The Houlihan et al. reference clearly does not teach or suggest two first MOSFETs having a common gate oxide film, let alone two first MOSFETs forming a CMOS pair having a common gate oxide film.

Further, the Houlihan et al. reference does not disclose the above feature on the same substrate as second and third MOSFETs having two different, but thicker gate oxide films, let alone that these second and third MOSFETs form a CMOS pair.

Indeed, the Examiner admits that the Houlihan et al. reference does not teach or suggest a CMOS pair.

The Baumann reference does not remedy these deficiencies.

While the Baumann reference appears to disclose a CMOS device with a PMOS device having a gate oxide that is thinner than the NMOS device, the Baumann reference does not teach or suggest two first MOSFETs forming a CMOS device with a common gate oxide film on the same substrate as another CMOS device with devices which not only have different gate oxide thicknesss, but also have gate oxide thicknesses which are thicker than the gate oxide film of the two first MOSFETs. Indeed, the Baumann reference would require that the two first MOSFETs also have two different thicknesses of gate oxide film.

Applicants respectfully request withdrawal of this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1 and 3-20, all the claims presently pending in the Application, are patentably distinct

over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 7/27/07

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